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	Filing Date	2004-03-11
	First Named Inventor	Cheng-Ku Chen
	Art Unit	2812
	Examiner Name	Cheung Lee
	Attorney Docket Number	TS03-375 (24061.518)

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CL	1	LEE, H.C., et al., "Reduction of Plasma Process-Induced Damage During Gate Poly Etching by Using a SiO ₂ Hard Mask", 3rd International Symposium on Plasma Process-Induced Damage, June 4-5, 1998, pages 72-75.	<input type="checkbox"/>
CL	2	NAKAI, S., et al., "A 100 nm CMOS Technology with "Sidewall-Notched" 40 nm Transistors and SiC-Capped Cu/VLK Interconnects for High Performance Microprocessor Applications", Symposium on VLSI Technology Digest of Technical Papers, 2002, pages 66-67.	<input type="checkbox"/>
CL	3	PIDIN, S., et al., "Experimental and Simulation Study on Sub-50 nm CMOS Design", Symposium on VLSI Technology Digest of Technical Papers, 2001, pages 35-36.	<input type="checkbox"/>
CL	4	TOMITA, K., et al., "Sub-1um ² High Density Embedded SRAM Technologies for 100nm Generation SOC and Beyond", Symposium on VLSI Technology Digest of Technical Papers, 2002, pages 14-15.	<input type="checkbox"/>
CL	5	TSUCHIYA, RYUTA, et al., "Femto-Second DMOS Technology with High-K Offset Spacer and SiN Gate Dielectric with Oxygen-Enriched Interface", Symposium on VLSI Technology Digest of Technical Papers, 2002, pages 150-151.	<input type="checkbox"/>
CL	6	WAKABAYASHI, H., et al., "A 0.10-um CMOS Device with a 40-nm Gate Sidewall and Multilevel Interconnects for System LSI", Symposium on VLSI Technology Digest of Technical Papers, 1999, pages 107-108.	<input type="checkbox"/>
CL	7	YANAGIYA, N., et al., "65nm CMOS Technology (CMOS5) with High Density Embedded Memories for Broadband Microprocessor Applications", Electron Devices Meeting, IEDM '02 Digest International, 2002, pages 57-60.	<input type="checkbox"/>

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